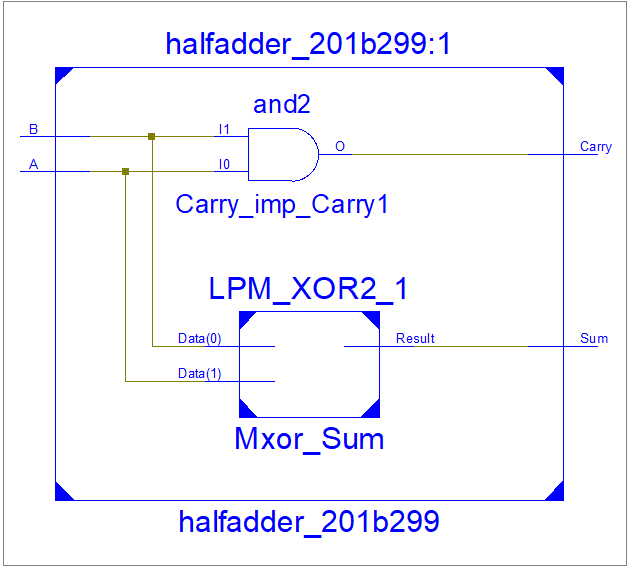
# Experiment 1

**Aim: Design of basic binary adders and subtractors.**

**Exercise 1:** Design half adder in **data flow style** of modeling.

**Design code:**

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity halfadder\_201b299 is

Port ( A : in STD\_LOGIC;

B : in STD\_LOGIC;

Sum : out STD\_LOGIC;

Carry : out STD\_LOGIC);

end halfadder\_201b299;

architecture Dataflow of halfadder\_201b299 is

begin

Sum <= A xor B;

Carry <= A and B;

end Dataflow;

**Test Bench:**